

High thermal conductivity AlN films for advanced 3D Chiplets

T. Takagi^{1*}, T. Ninomiya^{1*}, M. Niwa^{1*}, S. Obara², T. Momose², Y. Shimogaki², M. Nomura³, H. Fujioka³, M. Mori⁴, and T. Kuroda^{1*}

¹System Design Lab., ²Dept. of Materials Engineering, ³Inst. of Industrial Science, The University of Tokyo, Tokyo, Japan,

⁴Faculty of Adv. Sci. and Tech., Ryukoku University, Otsu, Japan, *RaaS, Tokyo Japan takagi@dlab.t.u-tokyo.ac.jp

Abstract

A novel “Cool 3D chiplet” concept is proposed, showcasing remarkable heat dissipation through the integration of aluminum nitride (AlN), an insulating material with high thermal conductivity. We conducted simulations analyzing the thermal impact of AlN as an interlayer dielectric (ILD) for the back-side power delivery network (BSPDN), a TSV insulating film, and a molding material for the packaging. Furthermore, we explored appropriate AlN deposition techniques for each application. The results demonstrate the feasibility of building advanced 3D chiplets with enhanced heat dissipation by employing the AlN in each layer that makes up the 3D chiplet, from the device level to the packaging level.

Keywords: 3DIC, BSPDN, TSV, HBM, chiplet, molding, AlN, heat dissipation, thermal conductivity, pulsed sputtering, thermal CVD, and aerosol deposition method.

Introduction

To achieve high performance and low power consumption, various 3DIC technologies are being developed at each technology level, including devices, stacked modules, and packaging. However, with the technology evolution, the energy density has increased and the temperature inside the chip has increased, which has become a serious problem. Recently, it has been reported to introduce high thermal conductivity dielectrics such as AlN and diamond in the bonding layer or back-end-of-line (BEOL) ILD to improve heat dissipation at the device level [1].

In this study, we proposed a novel “Cool 3D chiplet” that uses AlN not only at the device level but also in the stacked module and packaging to efficiently dissipate the heat generated inside the chip to the outside (Fig.1). Furthermore, we investigated the deposition methods of AlN films suitable for each application.

Thermal Simulations and Deposition Technologies

1. Device technology: BSPDN

BSPDN is effective in reducing area and IR drops as well as improving signal integrity and will be introduced at the 2 nm node and beyond. However, more efficient heat dissipation measures are essential for BSPDN because of its temperature increase caused by thin Si layer required to form high-density backside wiring [2].

We investigated the effect of introducing AlN as an ILD of back-side wiring layer and a bonding layer to the support Si (Fig.2). In this case, since AlN is used for the ILD of the power wiring layer, there is no negative effect due to its high dielectric constant. Depending on the thermal conductivity (κ) of the ILD, the peak temperature in the “Hot Spot” was lowered, lateral thermal diffusion was improved, and the temperature profile was comparable to that of conventional front-side PDN (FSPDN) using bulk Si substrate (Fig.3).

A pulsed sputtering deposition (PSD), which can suppress oxygen incorporation by depositing in UHV chamber and allows epitaxial growth of AlN even at room temperature [3], was considered for this application. It was confirmed that good

crystallinity with a high thermal conductivity of 54 W/m/K was obtained at 400°C deposition (Fig.4, 5).

2. Stacking technology: TSV insulator

Currently, 12 Hi High-Bandwidth Memory (HBM) is widely used for computing applications. The next generation HBM4 reportedly uses a hybrid bonding to lower thermal resistance than traditional bump connections, potentially enabling stacking up to 16 Hi including thermal properties [4].

To further improve a heat dissipation, we introduced AlN layer as a TSV insulator and investigated the possibility of 20 Hi HBM. Using the thermal simulation model (Fig.6), we investigated the relationship between the maximum temperature inside the chip (T_{j_max}) and the number of stacked layers when SiO₂ and AlN are used as a TSV insulator (Fig.7). As the number of layers increases, the temperature of the bottom layer furthest from the heat sink and laterally away from the TSV increases. Based on the thermal resistance (R_{th}) analysis that both the R_{th_TSV} and the R_{th_Si} have also large influence (Fig.8), we modified the HBM structure such as the TSV diameter, Si layer thickness, and TSV arrangement in addition to the TSV insulator. As a result, a low T_{j_max} comparable to 16 Hi in Fig.7 was found to be obtained (Fig.9).

A thermal CVD was selected as a deposition method of AlN film that can conformally deposit a film on the sidewall of a high aspect ratio TSV with a moderate deposition rate even at low temperatures. By using AlCl₃ as a source gas, columnar AlN polycrystals with relatively high thermal conductivity of 7.8 W/m/K at 650°C with conformal film formation on the side walls of high aspect ratio trenches could successfully be confirmed (Fig.10, 11). Further temperature reduction can be expected by using a highly reactive nitrogen source gas.

3. Packaging technology: Chiplet molding

Quasi-monolithic chip (QMC), where the chip is molded with SiO₂ instead of organic materials, was proposed for higher interconnect density and higher thermomechanical stability [5].

We proposed a dramatic improvement in heat dissipation at package level by using AlN instead of SiO₂ as a molding material. The effects of AlN were simulated using a Chiplet model, in which two stacked memory modules are mounted on top of a System-on-a Chip (SoC) (Fig.12). More than 20 deg T_{j_max} reduction was observed if the thermal conductivity of AlN was over 40 W/m/K (Fig.13).

An aerosol deposition method (ADM), a surface coating technique in which submicron-sized particles are sprayed onto a substrate to form a thick film at room temperature [6], was considered for this application. By adjusting the particle size, a formation of crystalline thick AlN film was confirmed (Fig.14) and good filling performance was achieved even for gaps with steps of 10 μ m and spaces of 10 μ m (Fig.15).

Conclusion

AlN is a promising high thermal conductivity insulator that can realize highly integrated high-performance 3D chiplets by its excellent heat dissipation capability in various types of the 3D chiplet as well as its appropriate deposition technologies.

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References

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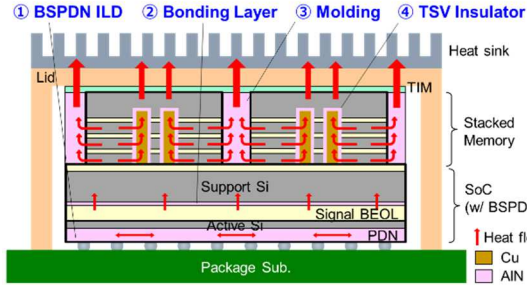


Fig.1 "Cool 3D chiplet" structure. AlN is adopted to BSPDN ILD, Bonding layer, TSV insulator and Molding.

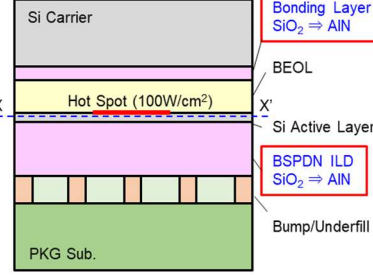


Fig.2 Thermal simulation model of BSPDN. AlN is adopted to the bonding layer and the BEOL ILD.

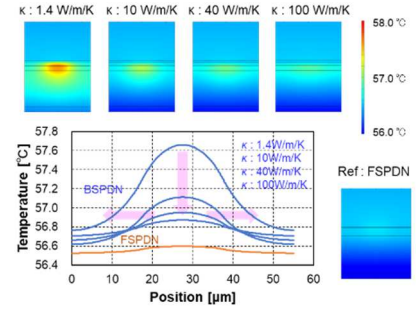


Fig.3 Temperature profiles of BSPDN for various κ . Peak temperature is decreased, and lateral heat dissipation is enhanced.

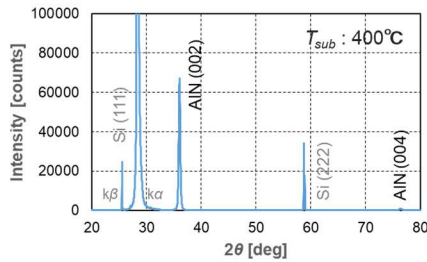


Fig.4 XRD spectrum of AlN films deposited by PSD at 400°C.

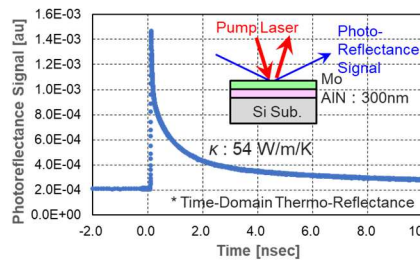


Fig.5 TDTR* signals of AlN films deposited by PSD at 400°C.

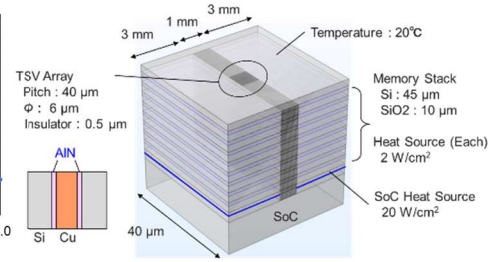


Fig.6 Thermal simulation model of HBM. AlN is adopted to the TSV insulator.

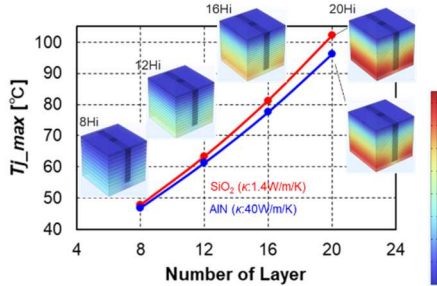


Fig.7 Stack number dependence of T_{j_max} . 5.9 deg reduction in AlN at 20Hi HBM

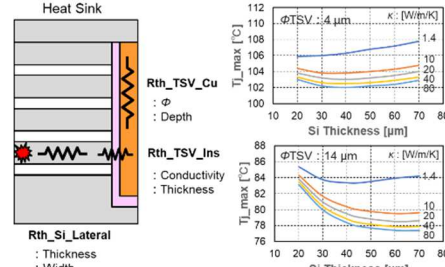


Fig.8 Consideration on thermal resistance. $R_{th_TSV_Cu}$ and $R_{th_Si_Lateral}$ are also important.

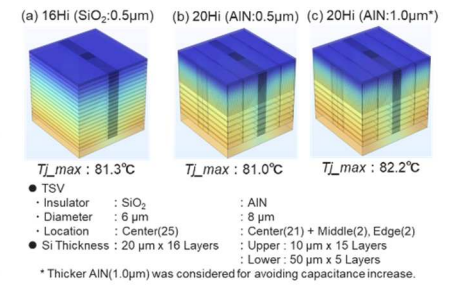


Fig.9 Temperature profiles of modified 20Hi HBM. T_{j_max} is comparable to 16Hi HBM shown in Fig.7.

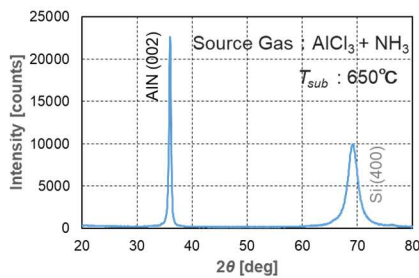


Fig.10 XRD spectrum of AlN film deposited by thermal CVD at 650°C

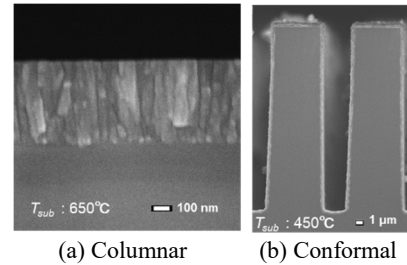


Fig.11 Cross section of AlN film deposited by thermal CVD.

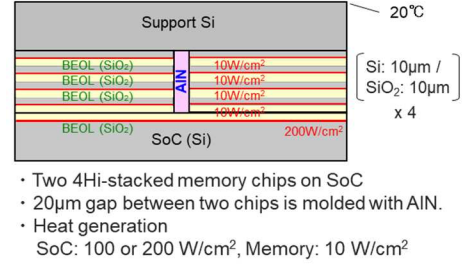


Fig.12 Thermal simulation model of chiplet molded with AlN.

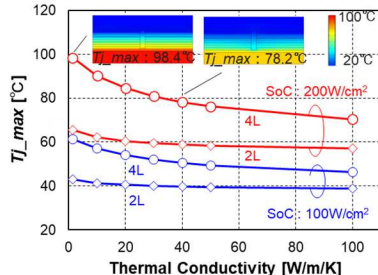


Fig.13 Thermal conductivity dependence of T_{j_max} . Large T_{j_max} reduction is obtained.

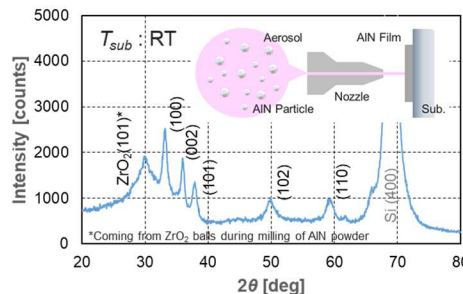


Fig.14 XRD spectrum of AlN films deposited by ADM at room temperature.

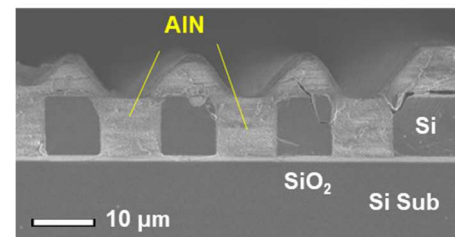


Fig.15 Cross section of AlN film deposited by ADM at room temperature. Gap is fully filled by AlN.